

SMC-01-808B

January 5, 2004

To: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/696,007 10/29/03

Ming-Fang Wang et al.

A NEW PROCESS FOR INTEGRATION OF A HIGH DIELECTRIC CONSTANT GATE INSULATOR LAYER IN A CMOS DEVICE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 29, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

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- U.S. Patent 5,972,762 to Wu, "Method of Forming MOSFETs with Recessed Self-Aligned Silicide Gradual S/D Junction, " discloses a method for forming recessd S/D silicide S/D junctions.
- U.S. Patent 5,970,329 to Cha, "Method of Forming Power Semiconductor Device Having Insulated Gate Electrodes, " discloses a recessed source and drain process.
- U.S. Patent 5,880,499 to Oyama, "Memory Cell of a Nonvolatile Semiconductor Device, " discloses a recessed source and drain.
- U.S. Patent 5,491,099 to Hsu, "Method of Making Silicided LDD with Recess in Semiconductor Substrate, "discloses a method for a silicided recessed LLD.

Stephen B. Ackerman,

Reg. No. 37761

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through it citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

DATE CONCIDERED

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